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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,977	03/16/2004	Chris Smith	CYPR-CD03005	3922

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EXAMINER	
TRA, ANH QUAN	
ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/802,977	SMITH ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/21/06 has been entered. A new ground of rejection is introduced as necessitated by amendment.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 6, 10, 11, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hara et al (USP 5994937) in view of Kwon (USP 5926045) and Mitsuishi (USP 6031366).

As to claim 1, Hara et al.'s figure 4 shows a timer circuit comprising an output stage (410, 412) coupled to a configurable delay element (402, 406); and a pull-down path (414) coupled to the output stage, the pull-down path coupled to receive a reference signal (Vref) that varies in proportion to temperature (figure 5) and wherein a delay through the timer circuit is inversely proportional to the temperature. The full down path functions as current source. Thus, figure 4 shows all limitations of claim 1 except for the pull-down path is a variable current source. However, Kwon's figure 2 shows a timer circuit having variable current source 20 coupled to output state 10 for adjusting the slew rate or frequency outputted from the output

state 10. Therefore, it would have been obvious to one having ordinary skill in the art to make Hara et al.'s pull-down path to be a variable current source for the purpose of having more flexibility of controlling the delay time of the delay circuit. The modified Hara et al.'s figure 4 fails to show the detail of the modified current source (414. It is noted that the current source 424 is also modified in order to ensure a balance output signal). However, Mitsushi's figure 3 shows a variable current source that compatible with Hara et al.'s pull-down stateand having simple structure. Therefore, it would have been obvious to one having ordinary skill in the art to use Mitsushi's variable current source for Hara et al.'s modified current source (transistor 414) for the purpose of saving cost. Thus, the modified Hara et al. reference further shows that the configurable delay element (402, 406) comprises plurality of selectively-activated component (Mitsuishi's IS1-Isn in the modified transistor 424, as noted above transistor 424 is also modified to become variable current source in order to ensure a balance output signal) operable to adjust a delay through the timer circuit.

As to claim 2, the modified Hara et al.'s figure 4 shows that the reference signal is derived from a band gap reference circuit (figure 5).

As to claim 3, the modified Hara et al.'s figure 4 shows that the reference signal is a VPTAT voltage signal (col. 4, lines 50-51).

As to claim 6, the modified Hara et al.'s figure 4 shows that the circuit for providing a selectable amount of pull down current comprises a plurality of gated pull-down circuits coupled in parallel wherein each gated pull-down circuit comprises a first switch (Sn) having controlled by a respective configuration bit and a series coupled second transistor (Mn) having a gate controlled by said reference signal. The modified Hara et al.'s figure 4 fails to shows that the switches S1-Sn are transistors. However, transistor using as a switch is well known in the art.

It would have been obvious to one having ordinary skill in the art to use transistors for switches S1-Sn for the purpose of saving space and cost.

Claims 10 and 11 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

As to claims 15 and 16, it is seen as an intended use for using the modified Hara et al.'s in a memory circuit.

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hara et al (USP 5994937) in view of Kwon (USP 5926045) and Mitsuishi (USP 6031366) and Saeki (USP 6388490).

As to claims 1 and 4, the modified Hara et al.'s figure 4 fails to show plurality of selectively active component that comprises a plurality of gated capacitors which can be selectively coupled to the output stage via a plurality of corresponding pass gates. However, Saeki's figure 3 shows a plurality of gated capacitors (CAP11-CAP15) which can be selectively coupled to output stage MP01-MN02 via a plurality of corresponding pass gates MN11-MN15 in order to adjust the delay outputted from the output stage. Therefore, it would have been obvious to one having ordinary skill in the art to add Saeki's delay adjusting circuit to Hara et al.'s output stage for the purpose of having more flexibility of controlling the delay of the signal outputted by the output stage.

As to claim 2, the modified Hara et al.'s figure 4 shows that the reference signal is derived from a band gap reference circuit (figure 5).

As to claim 3, the modified Hara et al.'s figure 4 shows that the reference signal is a VPTAT voltage signal (col. 4, lines 50-51).

As to claim 6, the modified Hara et al.'s figure 4 shows that the circuit for providing a selectable amount of pull down current comprises a plurality of gated pull-down circuits coupled

in parallel wherein each gated pull-down circuit comprises a first switch (Sn) having controlled by a respective configuration bit and a series coupled second transistor (Mn) having a gate controlled by said reference signal. The modified Hara et al.'s figure 4 fails to shows that the switches S1-Sn are transistors. However, transistor using as a switch is well known in the art. It would have been obvious to one having ordinary skill in the art to use transistors for switches S1-Sn for the purpose of saving space and cost.

Claims 10 and 11 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

As to claims 15 and 16, it is seen as an intended use for using the modified Hara et al.'s in a memory circuit.

As to claim 5, the modified Hara et al.'s figure 4 shows that the configurable delay element further comprises a plurality of configuration bits (inputs of Saeki's transistors MN11-MN15) each for controlling a respective pass gate.

As to claim 7, the modified Hara et al.'s figure 4 shows that the circuit for providing a selectable amount of pull down current comprises a plurality of gated pull-down circuits coupled in parallel wherein each gated pull-down circuit comprises a first switch (Sn) having controlled by a respective configuration bit and a series coupled second transistor (Mn) having a gate controlled by said reference signal. The modified Hara et al.'s figure 4 fails to shows that the switches S1-Sn are transistors. However, transistor using as a switch is well known in the art. It would have been obvious to one having ordinary skill in the art to use transistors for switches S1-Sn for the purpose of saving space and cost.

As to claim 8, the modified Hara et al.'s figure 4 shows that the plurality of selectively activated components comprises a plurality of gated capacitors which can be selectively coupled to the output stage via a plurality of corresponding pass gates.

As to claim 9, the modified Hara et al.'s figure 4 shows that the configurable delay element further comprises a plurality of configuration bits each for controlling a respective pass gate.

Claims 12-14 and 17-20 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

Response to Arguments

4. Applicant's arguments have been fully considered but they are not persuasive.

Applicant argues that Hara fails to teach the limitation "output stage". The Examiner respectfully disagrees. With broadest reasonable interpretation, "output stage" is a stage or circuit that outputs a signal. Clearly, Hara's circuit comprising 410 and 412 generates a signal at node between 410 and 412. Therefore, circuit comprising 410 and 412 can be considered as an output stage.

Applicant's further argues that the proposed modification under 35 U.S.C. 103(a) renders unsatisfactory for Hara intended purpose as well as changing its principle of operation. The Examiner respectfully disagrees. If one skilled in the art wished modified Hara's delay in order to optimum the circuit performance, he/she would have to employ Known and Mitsuishi's teaching to modify Hara's current source in order to get a desired delay.

Applicant further argues that there is no suggestion and motivation to combine the prior arts. The Examiner respectfully disagrees. It is not necessary that the cited references or prior arts actually suggest expressly or in so many words, the changes or improvements that applicant has made. The test for combining references is what the references as a whole would have suggested to one of ordinary skill in the art. In re Sheckier, 168 USPQ 716 (CCPA 1971) : In re McLaughlin 170 I USPQ 209 (CCPA 1971); In re Young 159 USPQ 725 (CCPA 1968).

Applicant further argues that the priors fail to teach the limitations of claim 17. However, the combination of Hara, Kwon, Mitsuishi and Sakei shows a circuit having variable current source (Hara with the current source of Kwon and Mitsuishi) receiving a second configuration bits, and variable delay capacitance (the modified Hara with Saeki's variable capacitance) receiving a first configuration bits. Further, Kwon teaches to vary a reference signal to control the delay time. The time that first and second configuration bits controlling the delay time is considered as the claimed "during configuration of said timer", and the time that the reference voltage controlling the delay is considered as the claimed "during operation of said timer".

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

June 7, 2007